**Lab Report 2**

**3)**

In section 3.1 of the lab we look at the latch affect of a basic SET/CLEAR NOR latch. From it was shown that a NOR latch activates on an active high, causing that state to either latch to Q if SET is pulled high, and NOT Q if CLEAR is pulled high. We also observed how when going from the invalid state of both SET and CLEAR high, to the no change state with both set low, it was random what state the latch would set itself too.

This latch configuration was then modified using two and gates to add an enable feature to the NOR latch. This allowed for selection of when the latch would operate, as the states of the SET and CLEAR pins would only be able to pass if the enable line was pulled high. This design was then again modified by connecting SET directly to CLEAR through a NOT gate. This final setup is a transparent D latch, as it only requires one input, and an enable line. This was then used to store the state of a square wave at a particular time by connecting the D pin to a square wave generator and the enable like to a pulse generator. When the enable line is pulsed, the current state of the square wave will be stored in the D flip-flop.

Next the properties of the 74HCT74 dual positive edge triggered flip-flop were investigated. It was observed that neither the SET or RESET lines were dependant on a clock signal, and could be used to modify the state of the flip-flop at any time. We also observed that the flip-flop was only responsive to changed on the LO -> HI edge of the clock pulse, meaning that if the clock were to remain high, there could be no changed made to the state of the flip-flop. It was also observed that the frequency of Q (the output of the flip-flop) was exactly half the frequency of the original clock pulse.

**3.5)**

Next the properties of the JK edge-triggered flip-flop were investigated. After wiring up the flipflop to logic level switched the following truth table can be constructed.

|  |  |  |  |
| --- | --- | --- | --- |
| **J** | **K** | **Q** | **NOT Q** |
| **1** | **1** | **switching** | **state** |
| **1** | **0** | **1** | **0** |
| **0** | **1** | **0** | **1** |
| **0** | **0** | **Stable** | **state** |

After connecting the oscilloscope to the clock input of the flip-flop, and the Q output of the flip-flop, it could be observed that the frequency of Q, was half the frequency of the CLK signal. This meant that if we set the CLK frequency to 10kHz, the frequency of Q would be 5kHz.

After using 4 of these JK flip-flops, we were able to combine them to create a ripple counter, with the output of the last flip-flip being the most significant bit.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pulses in | **QD** | **QC** | **QB** | **QA** |
| 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 1 |
| 3 | 0 | 0 | 1 | 0 |
| 4 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 0 |
| 6 | 0 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 0 |
| 8 | 0 | 1 | 1 | 1 |
| 9 | 1 | 0 | 0 | 0 |
| 10 | 1 | 0 | 0 | 1 |
| 11 | 1 | 0 | 1 | 0 |
| 12 | 1 | 0 | 1 | 1 |
| 13 | 1 | 1 | 0 | 0 |
| 14 | 1 | 1 | 0 | 1 |
| 15 | 1 | 1 | 1 | 0 |
| 16 | 1 | 1 | 1 | 1 |

By connecting the oscilloscope to the clock, and then each of the outputs respectively, we can see that each time the signal passes through another flip-flop the signal halves in frequency. This means that QA is ½ the CKL frequency, QB is ¼ the CKL frequency, QC is 1/8 the CLK frequency, and QD is 1/16 the CLK frequency.